Remarks

Reconsideration of this application as amended for prosecution is respectfully requested.

The Examiner objected to the drawings because of a typographical error in Figure 3, element 42. The attached amended drawing changes element 42 from "READ DATE" to "READ DATA."

The Examiner rejected claims 1-24. Claims 1-7 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,377,486 of Lee ("Lee"). Claims 8-16 and 9-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,201,739 of Brown ("Brown"). Claims 17-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Brown in view of U.S. Patent 6,189,070 of See ("See"). Claims 22-24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over See.

Please cancel claims 15-18 and 22-24. Please add new claims 25-29.

Applicants submit that amended claim 1 is not anticipated under 35 U.S.C. § 102(e) by Lee. Claim 1 includes the limitations:

> dividing the memory device into k partitions, wherein k is an integer greater than or equal to two;
> performing code operations from m code partitions out of k total partitions, wherein m is an integer greater than or equal to one; and
> performing data operations from n data partitions out of k total partitions through low level functions accessed from the code partitions at approximately the same time as the code operations are performed from the m code partitions, wherein n is an integer greater than or equal to one.

(Amended claim 1) (emphasis added).

In contrast, Lee discloses a block architecture of a cell array of a nonvolatile memory device. The memory device is divided into blocks. (Lee, column 5, lines 35-55). A block selection circuit selects one of the blocks of the memory cell array. Thus, the nonvolatile memory device of Lee supports a plurality of boot block architecture options for user selection. (Lee, column 3, lines 35-48). Applicants respectfully submit that the block architecture of Lee does not disclose performing data operations from n data partitions out of k total partitions of a memory device at approximately the same time as code operations are performed from m code partitions of the memory device.

Moreover, Lee does not disclose performing data operations from n data partitions out of k total partitions through low level functions accessed from the code partitions.

Given that claims 2-7 depend from claim 1, applicants submit that claims 2-7 are not anticipated under § 102(e) by the reference cited by the Examiner.

Applicants submit that claim 8 is not anticipated under 35 U.S.C. § 102(e) by Brown. Claim 8 includes the limitations:

> means for partitioning a memory device to enable multiple operations to be performed on a memory device at the same time; and
> means for tracking operations performed on the device to restore interrupted tasks.

(Claim 8) (emphasis added).

In contrast, Brown discloses "a method and apparatus for using a pin to preempt an operation in a nonvolatile writeable memory. Preempting an operation can be accomplished by either suspending the operation or aborting

the operation." (Brown, column 5, lines 22-25). Brown does not disclose performing multiple operations on the memory device at the same time, as set forth in claim 8. Further, Brown does not disclose partitioning a memory device.

Given that claims 9-10 depend from claim 8, applicants submit that claims 9-10 are not anticipated under § 102(e) by the reference cited by the Examiner.

Applicants submit that claim 11 is not anticipated under 35 U.S.C. § 102(e) by Brown. Claim 11 includes the limitations:

> a plurality of partitions;
> a status mode to provide partition status from the memory device;
> a read mode to read code and data from the memory device; and
> a write mode to write data to the memory device.

(Claim 11) (emphasis added).

In contrast, Brown discloses a "read status command" that makes it possible to determine whether a program cycle or an erase cycle is being performed by accessing the status of the flash EPROM. (Brown, column 9, lines 39-42). However, Brown neither discloses a memory array having a plurality of partitions nor a status mode to provide partition status from the memory device.

Given that claims 12-14 depend from claim 11, applicants submit that claims 12-14 are not anticipated under § 102(e) by the reference cited by the Examiner.

Applicants submit that claim 19 is not anticipated under 35 U.S.C. § 102(e) by Brown. Claim 19 includes the limitations:

> a memory device with k partitions, wherein k is an integer greater than or equal to two;
> low level functions to access the memory device;

and
a flag to indicate when a suspend operation has occurred.

(Claim 19) (emphasis added).

The Examiner states that Brown teaches a memory device with k partitions in figure 10. (3/13/03 office action, page 4). Applicants respectfully disagree. Figure 10 of Brown simply shows a flash EPROM that stores both code and data. (Brown, column 9, line 49). The flash EPROM of Brown does not have k partitions as set forth in claim 19.

Given that claims 20-21 depend from claim 19, applicants submit that claims 20-21 are not anticipated under § 102(e) by the reference cited by the Examiner.

Respectfully submitted,
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